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| 10/623,655 | 07/22/2003 | Tomoji Hamada | 2003-0996A | 4745 |

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| IM, JUNGHWA M | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2811 | |

DATE MAILED: 03/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EX

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/623,655 | HAMADA, TOMOJI | |
| | Examiner | Art Unit | |
| | Junghwa M. Im | 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *05 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 11, 13-15 and 17-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Hung et al. (US 5982250), hereinafter Hung.

Regarding claim 1, Fig. 3 of Hung shows a semiconductor apparatus comprising:

a semiconductor device [110];

a first dielectric board [228] surrounding the semiconductor device;

a second dielectric board [230] surrounding the semiconductor device and arranged on the first dielectric board;

a metal cover [204] on the second dielectric board and above the semiconductor device;

external electrodes [216 ];

upper wiring [112, 230] on the second dielectric board;

a first through-hole wiring [126] penetrating the first dielectric board and electrically connected with the external electrodes [col. 6, lines 9-14 or col. 5, lines 35-40];

a second through-hole wiring [126] penetrating the second dielectric board and connected with the semiconductor device [col. 6, lines 9-14]; and

an internal wiring [218; a conductive layer] inserted between the first dielectric

board and the second dielectric board;

wherein the semiconductor device is connected with the external electrodes via the first through-hole wiring, the second through-hole wiring and the internal wiring;

wherein the first through-hole wiring and the second through-hole wiring are electrically connected with the internal wiring [218; a conductive layer] while being away from each other.

Regarding claim 11, Fig. 3 of Hung shows said semiconductor device is connected to said upper wiring via a thin metal wire [114].

Regarding claims 13 and 17, Fig. 1 of Hung shows the whole external electrodes are completely arranged within an outer edge of the dielectric board [12].

Regarding claims 14 and 18, Fig. 1 of Hung shows a part of the external electrodes [216] is an external electrode for grounding, and an upper metal layer supplied with a ground potential via the external electrode for grounding is provided on an upper surface of the second dielectric board [col. 5, lines 24-46].

Regarding claims 15 and 19, Fig. 1 of Hung shows a part of the external electrodes [216] is an external electrode for grounding, and a lower metal layer supplied with a ground potential via the external electrode for grounding is provided on a lower surface of the first dielectric board [col. 5, lines 24-46].

## *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-3 and 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang in view of Karnezos (US 6020637).

Regarding claim 2, Fig. 3 of Hung shows the most aspect of the instant invention except "the second through-hole wiring is arranged more closely to the semiconductor device than the first through-hole wiring is." Fig. 1 of Karnezos shows a semiconductor device wherein the second through-hole wiring is arranged more closely to the semiconductor device than the first through-hole wiring is. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Karnezos into the device of Huang in order to have the second through-hole wiring arranged more closely to the semiconductor device than the first through-hole wiring for easier signal routing.

Regarding claim 3, Fig. 3 of Hung shows a semiconductor apparatus comprising:

the semiconductor is connected to the upper wiring via a thin metal wire [114, 118] connected to the semiconductor device.

Regarding claim 6, Fig. 1 of Hung shows a part of the external electrodes [216] is an external electrode for grounding, and an upper metal layer supplied with a ground potential via the external electrode for grounding is provided on an upper surface of the second dielectric board [col. 5, lines 24-46].

Regarding claim 7, Fig. 1 of Hung shows a part of the external electrodes [216] is an external electrode for grounding, and a lower metal layer supplied with a ground potential via the

external electrode for grounding is provided on a lower surface of the first dielectric board [col. 5, lines 24-46].

Claims 4-5 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hung and Karnezos as applied to claim 3 above, and further in view of Adachi et al. (US 6255739), hereinafter Adachi.

Regarding claim 4, the combined teachings of Hung and Karnezos show a metal plate [202] having the semiconductor device mounted thereon, however fails to show "the external electrodes and the metal plate being arranged on the plane." Fig. 6 of Adachi shows the external electrodes [11C] and the metal plate [12C] being arranged on the same plane. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Adachi into the device of Hung and Karnezos in order to have the external electrodes and the metal plate arranged on the same plane to reduce a package size.

Regarding claims 5 and 8, Fig. 1 of Hung shows the whole external electrodes are completely arranged within an outer edge of the dielectric board [12].

Regarding claim 9, Fig. 1 of Hung shows a part of the external electrodes [216] is an external electrode for grounding, and an upper metal layer supplied with a ground potential via the external electrode for grounding is provided on an upper surface of the second dielectric board [col. 5, lines 24-46].

Regarding claim 10, Fig. 1 of Hung shows a part of the external electrodes [216] is an external electrode for grounding, and a lower metal layer supplied with a ground potential via the

external electrode for grounding is provided on a lower surface of the first dielectric board [col. 5, lines 24-46].

Claims 12 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hung in view of Adachi et al. (US 6255739), hereinafter Adachi.

Regarding claims 12 and 16, Fig. 1 of Hung shows a metal plate [202] having the semiconductor device mounted thereon, however fails to show the external electrodes and the metal plate being arranged on the plane. Fig. 6 of Adachi shows the external electrodes [11C] and the metal plate [12C] being arranged on the same plane. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Adachi into the device of Hung in order to have the external electrodes and the metal plate arranged on the same plane to reduce a package size.

***Response to Arguments***

Applicant's arguments filed January 6, 2005 have been fully considered but they are not persuasive. The rejection stands, modified only to accommodate the amendments made to the claims by Applicant. New rejections are made in response to Applicant amended claims.

Applicant argues that "[c]laim 1 has been amended to included the additional limitation of upper wiring on the second dielectric board, wherein the second through-hole wiring is electrically connected with the upper wiring." However, the language of the rejection has been modified to meet the amended claim limitations. Therefore, Hung still anticipates the claims of the instant invention.

*Conclusion*

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jmi

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SPE TC 2800